IN THE SPECIFICATION

Page 14, lines 11-13, delete "Once the controls signal has selected a given segment, the control signal remains high and no transition of control is";

Page 13, line 26, change "520" to -- 510 –; so that the paragraph on pages 13 and 14 appears as follows:

– When segment driver 450 is activated, the active global word line will provide access to a local word line for reading or writing to a specific memory location. This process is accomplished as follows. The memory chip is activated by supplying a signal to the CLOCK input of segment driver 450. The control (CTL) or segment signal is used to select one of the memory subarrays or segments for reading or writing. In circuit 500, CTL is also supplied as an input signal to pulse discharge circuit 310. After a small propagation delay, the control circuit (not shown) creates a decoding signal DECODE that activates the appropriate subarray by connecting select line 460 to ground. When all three of the input signals to segment driver 450 are active, select line 460 is used to discharge the accumulated charge on the SOI transistors. This time, instead of discharging through segment driver 450 as shown in FIG. 4, the accumulated charge is dissipated through a pull-down transistor in inverter 624 which is located in pulse discharge circuit 310. This is accomplished as follows. In normal operation, to select a given memory subarray, the CTL signal for that subarray

transitions from low to high. This CTL signal is also supplied to pulse discharge circuit 310 as an input signal. After a brief propagation delay through a delay element (invertors or other circuit device), circuit node 621 will transition from high to low. Circuit node 622 will generate a negative pulse and, after passing through an inverter, becomes a positive pulse at node 623. The positive signal or pulse applied to transistor 625 activates transistor 625 which, in turn, provides a path for discharging the word line drivers of memory circuit 500 through inverter 624. The pulse discharge signal generated by pulse generator 510 is the output signal from the pulse discharge circuit and, in a preferred embodiment of the present invention, is supplied to the memory subarray just prior to the selection of the subarray for access. This means that the charge accumulated on the bodies of the SOI transistors has already been discharged when the request to access the subarray is received. By removing the charge before the first access occurs, the access time to the subarray is greatly enhanced. While it is possible to provide a discharge pulse prior to every access, this is not necessary. Once the initial accumulation of charge has been dissipated, as long as subsequent accesses are to the same subarray, there will not be very much charge accumulated in the subarray. By discharging the subarray prior to the first access only, the additional power requirements necessary to implement the invention are minimal.